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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,257	06/26/2003	Yeu Wen Lee	ONS00461	3696
7590	09/25/2006		EXAMINER	
James J. Stipanuk Semiconductor Components Industries, L.L.C. Patent Administration Dept - MD/A700 P.O. Box 62890 Phoenix, AZ 85082-2890			STAICOVICI, STEFAN	
			ART UNIT	PAPER NUMBER
			1732	
			DATE MAILED: 09/25/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,257	LEE ET AL.	
	Examiner Stefan Staicovici	Art Unit 1732	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 17 July 2006.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1,2,4-13,15,16,21,23 and 24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-2, 4-13, 15-16, 21 and 23-24 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application
- 6) Other: _____.

DETAILED ACTION

Terminal Disclaimer

1. The terminal disclaimer filed on July 17, 2006 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US Patent No. 6,835,580 has been reviewed and is not accepted.
2. An attorney or agent, not of record, is not authorized to sign the terminal disclaimer in the capacity as an attorney or agent acting in a representative capacity as provided by 37 CFR 1.34
(a). See 37 CFR 1.321(b) and/or (c).

Response to Amendment

3. Applicants' amendment filed July 17, 2006 has been entered. Claims 1-2, 4-13, 15-16, 21 and 23-24 are pending in the instant application.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned

with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-2, 4-13, 15-16, 21 and 23-24 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 6,835,580 in view of JP 2001-230520 and Takahashi *et al.* US Patent No. 5,766,972).

Claims 1-20 of U.S. Patent No. 6,835,580 teach the basic claimed process including, attaching (bonding) an electronic chip having a bond pad on an outer surface to a lead-frame structure, attaching a conductive stud to said bond pad, encapsulating said electronic chip, forming an opening in the upper surface to expose the conductive stud, forming a nickel barrier layer on the conductive stud and attaching a solder bump to the nickel barrier layer.

Regarding claims 1-2, 7, 9, 21 and 24, Claims 1-20 of U.S. Patent No. 6,835,580 do not teach that said mold has a blocking device, such as a pin, that contacts said conductive bump and that upon injection molding openings are formed in the encapsulating material. JP 2001-230520 teaches an injection molding process for making a plurality of openings and through-holes (recessed openings) at selected locations of a resulting molded article by using a mold having a plurality of protrusions (11) and pins (12) (see Abstract and, Figures 1b and 1c). Takahashi *et al.* ('972) teach a process for encapsulating a semiconductor device including, attaching (bonding) conductive bumps (30a) using bonding pads (31) to a chip structure (30) to form a semiconductor assembly (DCA), placing said DCA device into a mold cavity such that the top surface said conductive bumps (30a) are flush with said mold surface, applying pressure to maintain full contact at the interface between said mold and said conductive bumps (30a),

injection molding a resin material to encapsulate said DCA device and also form openings where said conductive bumps are present in order for solder balls (30b) to be attached (see col. 8, line 59 through col. 9, line 48 and Figures 8-11). Therefore, in view of the teachings of Takahashi *et al.* ('972) showing a desirability to form openings where said conductive bumps are present, it would have been obvious for one of ordinary skill in the art to have provided a mold having a plurality of protrusions and pins as taught by JP 2001-230520 in the process of Claims 1-20 of U.S. Patent No. 6,835,580 because, Takahashi *et al.* ('972) specifically teach a desirability to form openings where said conductive bumps are present without the need of an extra step of removing resin material, hence providing for an improved process. It is submitted that said conductive bumps formed by the process of Claims 1-20 of U.S. Patent No. 6,835,580 in view of JP 2001-230520 and in further view of Takahashi *et al.* ('972) are recessed within the resulting opening because JP 2001-230520 specifically teaches making a plurality of openings and through-holes (recessed openings) at selected locations.

Further regarding claims 1-2, 9 and 24, although Claims 1-20 of U.S. Patent No. 6,835,580 in view of JP 2001-230520 and in further view of Takahashi *et al.* ('972) do not teach a removable pin, it is noted that whether said pin is fixed or removable merely providing a component that is separable rather than integral without providing any unexpected results. Therefore, it would have been obvious for one of ordinary skill in the art to provide removable pins to the mold in the process of Claims 1-20 of U.S. Patent No. 6,835,580 in view of JP 2001-230520 and in further view of Takahashi *et al.* ('972) because of known advantages such as improved versatility, design flexibility and ease of operation and maintenance, hence providing for an improved process.

Specifically regarding claims 4 and 8, Claims 1-20 of U.S. Patent No. 6,835,580 teaches the use of bonding pads to attach conductive balls or bumps to said electronic chip and subsequently attaching solder balls to said conductive balls or bumps through said openings.

Further regarding claim 7 and in regard to claims 5, 10 and 24, Takahashi *et al.* ('972) teach that conductive bumps of a DCA device have chamfered edges and a flat surface. It is noted that JP 2001-230520 teaches protrusions that have a flat surface (see Figure 1b). Therefore, in view of Takahashi *et al.* ('972) teaching that conductive bumps of a DCA device have chamfered edges and a flat surface, it would have been obvious for one of ordinary skill in the art to have provided pins having chamfered edges and a flat surface in the process of Claims 1-20 of U.S. Patent No. 6,835,580 in view of JP 2001-230520 and in further view of Takahashi *et al.* ('972) because of the known principle that the mold surface must match the surface of the molded article, hence only pins having chamfered edges and a flat surface are able to form openings that are complementary to conductive bumps having chamfered edges and a flat surface and as such for the invention of Claims 1-20 of U.S. Patent No. 6,835,580 in view of JP 2001-230520 and in further view of Takahashi *et al.* ('972) to function as described.

In regard to claims 6 and 13, Claim 14 of U.S. Patent No. 6,835,580 teach a MOSFET device.

Further regarding claim 21 and, in regard to claims 11-12 and 15-16, Claim 15 of U.S. Patent No. 6,835,580 teach a flag portion.

Regarding claim 23, Claims 1-2 of U.S. Patent No. 6,835,580 teach a nickel barrier layer.

Response to Arguments

6. Applicant's arguments filed July 17, 2006 have been considered.
7. In view of the amendment filed July 17, 2006 the rejection of claims 1-2, 4-13, 15-16, 21 and 23-24 under 35 U.S.C. §103 has been withdrawn.
8. With regards to the nonstatutory double patenting rejection of claims 1-2, 4-13, 15-16, 21 and 23-24, the rejection has been maintained because the terminal disclaimer filed July 17, 2006 has not been accepted. That is, the attorney or agent, signing the terminal disclaimer filed July 17, 2006 is not of record, hence is not authorized to sign the terminal disclaimer in the capacity as an attorney or agent acting in a representative capacity as provided by 37 CFR 1.34 (a). See 37 CFR 1.321(b) and/or (c).
9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Staicovici, Ph.D. whose telephone number is (571) 272-1208. The examiner can normally be reached on Monday-Friday 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christina Johnson, can be reached on (571) 272-1176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stefan Staicovici, PhD


Primary Examiner 9/24/06

AU 1732

September 22, 2006